BE Semester- III (Instrumentation & Control) Question Bank

(DIGITAL TECHNIQUES)

All questions carry equal marks(10 marks)

Q.1	Convert the following
	  i. hexadecimal equivalent of the decimal number 256.
	  ii. octal equivalent of the decimal number 64
	  iii. decimal equivalent of $(123)_9$
	  iv. the decimal number 214 to hexadecimal
	  v. 378.93_{10} to octal

Q.2	Convert A3BH and 2F3H into binary and octal respectively

Q.3	Reduce the expression:
	  I. $A[B + \bar{C}(\overline{AB + A\bar{C}})]$
	  II. $(\overline{A + \overline{BC}})\,(A\bar{B} + ABC)$

Q.4	Simplify using k-map to obtain a minimum pos expression: (A' + B'+C+D) (A+B'+C+D) (A+B+C+D') (A+B+C'+D') (A'+B+C'+D') (A+B+C'+D)
Q.5	Reduce the following equation using Quine Mc Clucky method of minimization F (A,B,C,D) = _m(0,1,3,4,5,7,10,13,14,15)
Q.6	Using a K-Map, Find the MSP form of F= _ (0-3, 12-15) + _d (7, 11)
Q.7	Using a K-Map ,Find the MSP from of F= _(0,4,8,12,3,7,11,15) +_d(5)
Q.8	State and Prove Demorgan's theorem
Q.9	Define half adder and full adder. Design full adder using half adder.
Q.10	Define half subtractor and full subtractor. Design full subtractor using half subtractor.
Q.11	Explain BCD-to-Seven segment decoder.
Q.12	Define comparator. Explain 4-bit magnitude comparator with logic diagram.
Q.13	Draw and design 2-bit magnitude comparator circuit.
Q.14	Design a BCD adder using two 4 bit address.
Q.15	Distinguish between a multiplexer and a demultiplexer.
Q.16	Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input numbers.
Q.17	What is a PLA? Explain it with example.
Q.18	Distinguish between combinational and sequential switching circuits.
Q.19	Briefly explain the conversion of flip-flops with block diagram and also explain steps of conversion of flip-flop with an example.
Q.20	Discuss the applications of flip-flops.
Q.21	Explain position edge-triggered D flip-flop.

Q.22	Explain Master-Slave (pulse-triggered) S-R flip-flop.
Q.23	Explain triggering of flip-flops with waveform.
Q.24	Explain the gated SR latch flip-flop.
Q.25	Design SR flip-flop using JK flip-flop.
Q.26	For the clocked JK flip-flop writ the state table, draw the state diagram and the state equation.
Q.27	For the clocked D flip-flop writ the state table, draw the state diagram and the state equation.
Q.28	Explain with logic diagram of 4-bit serial-in, serial-out, shift register.
Q.29	Explain with logic diagram of 4-bit serial-in, parallel-out, shift register.
Q.30	Explain with logic diagram of 4-bit parallel-in, serial-out, shift register.
Q.31	Explain with logic diagram of 4-bit bidirectional shift register.
Q.32	Distinguish between asynchronous and synchronous counters.
Q.33	Explain 4-bit ring counter with circuit diagram and waveforms.
Q.34	Explain 4-bit Johnson counter with circuit diagram and waveforms.
Q.35	Design and implement a synchronous 3-bit up/down counter using JK flip-flops.
Q.36	Design and implement a synchronous BCD counter using JK filp-flops.

Q.37	Define the following terms
	    I. threshold voltage
	   II. propagation delay
	  III. power dissipation
	  IV. fan-in
	    V. fan-out

Q.38	With the help of a neat diagram, explain the working of a two-input TTL NAND gate.

Q.39	With the help of a neat diagram, explain the working of any two
	    I. a CMOS inverter,
	   II. a two input CMOS NAND gate
	  III. a two input CMOS NOR gate

Q.40	What do you mean by interfacing? Why it is required? Explain CMOS to TTL interfacing.